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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TANG, KAREN C	
ART UNIT	**PAPER NUMBER**
2151	

DATE MAILED: 09/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/978,475	ROSE ET AL.	
	Examiner	Art Unit	
	Karen C. Tang	2151	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 and 7 are unclear and ambiguous to Examiner, but due to the examining purpose, Examiner has decided to go with the Independence Claim 1, which, "the second period time is subsequent to the first period of time".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 11, 12, 18-20, 25, and 26 rejected under 35 U.S.C. 102(e) as being anticipated by Holden et al hereinafter Holden (US 6,147,997).

1. Referring to Claims 1 and 18, Holden discloses a transmitting device transmitting data at a first non-zero rate to a memory for storage therein during a first period of time (refer to Col 2, Lines 30-67, it is inherent that the device transmit the first rate, THEN

reduce the rate, then transfer the SECOND reduced rate, which the device are transfer first and second rate at different point in time); the transmitting device transmitting data at a second non-zero rate to the memory for storage therein during a second period of time (refer to Col 2, Lines 30-67); wherein the second period of time is subsequent to the first period of time (it is inherent that the device transmit the first rate, THEN reduce the rate, then transfer the SECOND reduced rate, which the second period of time is following the first period of time) and wherein the second non-zero rate is greater than or less than the first non-zero rate (refer to Col 2, Lines 45-60).

2. Referring to Claims 2, 11, 19, and 25, Holden discloses wherein the memory device comprises a FPO buffer (refer to Col 4, Lines 1-25):

3. Referring to Claims 3, 12, 20, and 26, Holden discloses wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein (refer to Col 3, Lines 25-67 and Col 4, Lines 1-40).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 21 rejected under 35 U.S.C. 103(a) as being unpatentable over Holden et al hereinafter Holden (US 6,147,997) in view of Shinohara (US 6,122,251).

1. Referring to Claims 4 and 21, Holden discloses a transmit signal (refer to Col 4, lines 15-55); first rate and second rate (refer to Col 4); and a memory device (refer to Col 2); Holden does not expressly indicate discloses further comprising: generating a rate control signal to the transmitting device instructing the transmitting device to stop transmitting data at the first non-zero rate and start transmitting data at the second non-zero rate; transmitting the rate control signal to the transmitting device, wherein the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal.
Shinohara expressly indicate: generating a rate stop control signal (refer to Col 7, Lines 30-67); transmitting the rate control signal to the transmitting device, wherein the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal (refer to Col 7, and Col 8).
At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Holden and Shinohara because the inventions are all based on ATM switching.

The suggestion/motivation for doing so would have been that it would have been that by implementing a control signal, it is easier for user to have more control and makes the system more dynamic.

Claims 5-10, 13, 14-17, 22-24, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holden et al hereinafter Holden (US 6,147,997) in view of Shinohara (US 6,122,251) in further view of Ito et al hereinafter Ito (US 5,539,747)

1. Referring to Claims 5, 13, 22, and 27, Holden generating first data quantity value (refer to Col 2), representing a quantity of data stored in the memory device at a first point in time (FIFO, refer to Col 4);
Holden does not expressly indicate control signal being generated.
Shinohara discloses control signal being generated (refer to Col 7, Lines 30-67).
At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Holden and Shinohara because the inventions are all based on ATM switching.
The suggestion/motivation for doing so would have been that it would have been that by implementing a control signal, it is easier for user to have more control and makes the system more dynamic.
Neither Holden nor Shinohara disclose the data quality value to a predetermine value.
Ito discloses comparing the first data quantity value to a first predetermined value (refer to Col 14);

At the time of the invention, it would have been obvious or ordinary skill in the art to combine Holden, Shinohara and Ito because they are all focus their invention environment on switching unit.

The suggestion/motivation for doing so would have been that Shinohara compares the queue length and predetermine value. Which, the queue value can be formed by the counter of quality data within the buffer.

2. Referring to Claims 6 and 23, Holden discloses first data rate (refer to Col 4) and a memory (FIFO, refer to Col 4).

Holden does not expressly indicate control signal being generated.

Shinohara discloses control signal being generated (refer to Col 7, Lines 30-67).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Holden and Shinohara because the inventions are all based on ATM switching.

The suggestion/motivation for doing so would have been that it would have been that by implementing a control signal, it is easier for user to have more control and makes the system more dynamic.

Neither Holden nor Shinohara disclose the first data quality value to a first predetermine value.

Ito discloses comparing the data quantity value to a predetermined value (refer to Col 13 and 14);

At the time of the invention, it would have been obvious or ordinary skill in the art to combine Holden, Shinohara and Ito because they are all focus their invention environment on switching unit.

The suggestion/motivation for doing so would have been that Shinohara compares the queue length and predetermine value. Which, the queue value can be formed by the counter of quality data within the buffer.

3. Referring to Claims 7 and 15, Holden discloses second data rate (refer to Col 4) and a memory (FIFO, refer to Col 4).

wherein the second point in time is prior to the first point in time (Examiner interprets that the first point is before the second point in time, refer to Col 2, Lines 30-67, it is inherent that the device transmit the first rate, THEN reduce the rate, then transfer the SECOND reduced rate, which the device are transfer first and second rate at different point in time); wherein the rate control signal is generated if the first data quantity value is not equal to the second data quantity value (it is inherent that it will not be equal because Holden already indicate that the first data is not equal to the second data rate, thus the queuing length is longer.).

Holden does not expressly indicate control signal being generated.

Shinohara discloses control signal being generated (refer to Col 7, Lines 30-67).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Holden and Shinohara because the inventions are all based on ATM switching.

The suggestion/motivation for doing so would have been that it would have been that by implementing a control signal, it is easier for user to have more control and makes the system more dynamic.

Neither Holden nor Shinohara disclose comparing the data quality value to a predetermine value.

Ito discloses comparing the first data quantity value to a first predetermined value (refer to Col 13 and 14);

At the time of the invention, it would have been obvious or ordinary skill in the art to combine Holden, Shinohara and Ito because they are all focus their invention environment on switching unit.

The suggestion/motivation for doing so would have been that Shinohara compares the queue length and predetermine value. Which, the queue value can be formed by the counter of quality data within the buffer.

Neither Holden nor Shinohara disclose the first data quality value to a first predetermine value.

Ito discloses comparing the first data quantity value to a second data quality value (Examiner interprets the second data quality value is the predetermine value, refer to Col 13 and 14);

At the time of the invention, it would have been obvious or ordinary skill in the art to combine Holden, Shinohara and Ito because they are all focus their invention environment on switching unit.

The suggestion/motivation for doing so would have been that Shinohara compares the queue length and predetermine value in FIFO buffer (refer to Col 10). Which, the queue value can be formed by the counter of quality data within the buffer.

4. Referring to Claim 8, Holden teaches first data rate and second data rate (refer to Col 4)

Neither Holden nor Shinohara disclose indicate wherein generating the first data quantity value comprises:

generating total data input count at the first point in time, wherein the total data input count represents a quantity of data input to the memory device during a period of time ending in the first point in time;

Ito discloses generating total data input count at the first point in time, wherein the total data input count represents a quantity of data input to the memory device during a period of time ending in the first point in time (refer to Col 15 and 16 and 13);

Neither Holden nor Shinohara disclose generating total data output count at the first point in time, wherein the total data output count represents a quantity of data output from the memory device during the period of time ending in the first point in time;

Ito discloses generating total data output count at the first point in time, wherein the total data output count represents a quantity of data output from the memory device during the period of time ending in the first point in time (refer to Col 15);

Neither Holden nor Shinohara disclose subtracting the total data output count from total data input count.

Ito discloses subtracting the total data output count from total data input count (refer to Col 15 and 16).

At the time of the invention, it would have been obvious or ordinary skill in the art to combine Holden, Shinohara and Ito because they are all focus their invention environment on switching unit.

The suggestion/motivation for doing so would have been that Shinohara compares the queue length and predetermine value in FIFO buffer (refer to Col 10). Which, the queue value can be formed by the counter of quality data within the buffer.

5. Referring to Claims 9 and 17, Holden discloses (first and second rate, and the two rates are different, refer to Col 4).

Holden wherein the second non-zero rate is greater than the first non-zero rate if the second data quantity value is less than the first data quantity value, and wherein the second non-zero rate is less than the first non-zero rate if the second data quantity value is less than the first data quantity value (it is inherent that the count depends on the number of data input to the memory device, so, if the data rate is higher, then the number of data input is high as well).

6 Referring to Claim 14, Holden discloses circuits (refer to Col 1 and 3)

Neither Holden nor Shinohara expressly indicate a plurality of comparing circuits, each one of which is configured to compare the first data quantity value to a respective one of a plurality of predetermined values, wherein the first comparing circuit is one of the

plurality of comparing circuits, and wherein the first predetermined value is one of the plurality of first predetermined values', wherein the circuit generates the rate control signal in response to comparing the first data quantity value to the plurality of predetermined values.

Ito discloses a plurality of comparing circuits, each one of which is configured to compare the first data quantity value to a respective one of a plurality of predetermined values, wherein the first comparing circuit is one of the plurality of comparing circuits, and wherein the first predetermined value is one of the plurality of first predetermined values', wherein the circuit generates the rate control signal in response to comparing the first data quantity value to the plurality of predetermined values (refer to Col 13, 15, 16, and 17).

At the time of the invention, it would have been obvious or ordinary skill in the art to combine Holden, Shinohara and Ito because they are all focus their invention environment on switching unit.

The suggestion/motivation for doing so would have been that Shinohara compares the queue length and predetermine value in FIFO buffer (refer to Col 10). Which, the queue value can be formed by the counter of quality data within the buffer.

7. Referring to Claim 16, Holden does not expressly indicate the chips, and it is inherent that chips comprises many circuits (refer to Col 1 and 3).

8. Referring to Claims 10 and 24, Holden discloses a memory device configured to receive data from a transmitting device for storage therein (refer to Col 4);

wherein the second non-zero rate is greater than or less than the first non-zero rate (refer to Col 2, Lines 45-60);

Holden does not expressly indicate a first means for generating and transmitting a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non- zero rate and to begin transmitting data to the memory device at a second non- zero rate;

Shinohara expressly indicate: generating a rate stop control signal (refer to Col 7, Lines 30-67); transmitting the rate control signal to the transmitting device, wherein the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal (refer to Col 7, and Col 8).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Holden and Shinohara because the inventions are all based on ATM switching.

The suggestion/motivation for doing so would have been that it would have been that by implementing a control signal, it is easier for user to have more control and makes the system more dynamic.

Conclusion

A shortened statutory period for reply to this Office action is set to expire THREE MONTHS from the mailing date of this action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Karen C. Tang whose telephone number is (571)272-3116. The examiner can normally be reached on M-F 7 - 3.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarni Maung can be reached on (571)272-3939. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KT

ZARNI MAUNG
SUPERVISORY PATENT EXAMINER